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(FILE 'USPAT' ENTERED AT 15:56:02 ON 14 NOV 96)

SET PAGE SCROLL

L1 23 S 395/292/CCLS

L2 247 S 395/200.15,825,826,860/CCLS

L3 77 S 395/307/CCLS

L4 280 S 395/497.01,497.02,478/CCLS

L5 359 S (VARIABLE (5A) LENGTH (5A) (QUEUE# OR BUFFER#))

L6 0 S L1 AND L2 AND L3 AND L4

L7 618 S L1 OR L2 OR L3 OR L4

L8 5 S L5 AND L7

L9 64 S (NEST? OR MULTILEVEL) (5A) (QUEUE# OR BUFFER#)

L10 1 S L7 AND L9

L11 1 S L5 AND L9

L12 2819 S (BUS (5A) (SPEED OR THROUGHPUT))

L13 15 S L5 AND L12

L14 0 S L5 (P) L12

L15 4 S L9 AND L12

L16 2 S (PRIORIT? (5A) NON-FIFO)

L17 971 S 395/250/CCLS

L18 18 S L5 AND L17

L19 3 S L9 AND L17

L20 45 S KRICK?/XA

L21 3 S L17 AND L20

L22 52255 S (CONCURRENT? OR SIMULTANEOUS?) (5A) (PROCESS? OR OPERATION#

L23 219 S L17 AND L22

L24 21 S L12 AND L23

L25 27 S SUB-QUEUES

L26 155 S (BUFFER? OR QUEUE?) (5A) (PRIORITY (3A) LEVEL#)

L27 16 S L12 AND L26

FILE 'JPOABS' ENTERED AT 17:29:03 ON 14 NOV 96

L28 78 S L5

L29 21 S L9

L30 826 S L12

L31 0 S L16

L32 10312 S L22

L33 0 S L25

L34 15 S L30 AND L32

FILE 'USPAT' ENTERED AT 17:36:08 ON 14 NOV 96

L35 75 S (BUS AND (SPEED OR THROUGHPUT))/TI

L36 990 S 395/250,827/CCLS

L37 3 S L35 AND L36

US PAT NO: 5,572,682 [IMAGE AVAILABLE] L18: 1 of 18
TITLE: Control logic for a sequential data buffer using byte read-enable lines to define and shift the access window

US PAT NO: 5,563,920 [IMAGE AVAILABLE] L18: 2 of 18
TITLE: Method of processing variable size blocks of data by storing numbers representing size of data blocks in a fifo

US PAT NO: 5,442,756 [IMAGE AVAILABLE] L18: 3 of 18
TITLE: Branch prediction and resolution apparatus for a superscalar computer processor

US PAT NO: 5,412,805 [IMAGE AVAILABLE] L18: 4 of 18
TITLE: Apparatus and method for efficiently allocating memory to reconstruct a data structure

US PAT NO: 5,402,361 [IMAGE AVAILABLE] L18: 5 of 18
TITLE: Apparatus for method for logging, storing, and redirection of process related non-densitometric data generated by color processing equipment for use by an off site host computer

US PAT NO: 5,396,595 [IMAGE AVAILABLE] L18: 6 of 18
TITLE: Method and system for compression and decompression of data

US PAT NO: 5,313,582 [IMAGE AVAILABLE] L18: 7 of 18
TITLE: Method and apparatus for buffering data within stations of a communication network

US PAT NO: 5,224,212 [IMAGE AVAILABLE] L18: 8 of 18
TITLE: Asynchronous operation in a database management system

US PAT NO: 5,214,783 [IMAGE AVAILABLE] L18: 9 of 18
TITLE: Device for controlling the enqueuing and dequeuing operations of messages in a memory

US PAT NO: 5,175,819 [IMAGE AVAILABLE] L18: 10 of 18
TITLE: Cascadable parallel to serial converter using tap shift registers and data shift registers while receiving input data from FIFO buffer

US PAT NO: 5,079,693 [IMAGE AVAILABLE] L18: 11 of 18
TITLE: Bidirectional FIFO buffer having reread and rewrite means

US PAT NO: 4,839,791 [IMAGE AVAILABLE] L18: 12 of 18
TITLE: Input/output buffer system

US PAT NO: 4,750,149 [IMAGE AVAILABLE] L18: 13 of 18
TITLE: Programmable FIFO buffer

US PAT NO: 4,396,995 [IMAGE AVAILABLE] L18: 14 of 18
TITLE: Adapter for interfacing between two buses

US PAT NO: 4,377,853 [IMAGE AVAILABLE] L18: 15 of 18
TITLE: Peripheral controller with segmented memory buffer for interfacing 80 column card reader with host computer

US PAT NO: 4,371,927 [IMAGE AVAILABLE] L18: 16 of 18
TITLE: Data processing system programmable pre-read capability

US PAT NO: 4,322,792 [IMAGE AVAILABLE] L18: 17 of 18
TITLE: Common front-end control for a peripheral controller connected to a computer

US PAT NO: 4,313,162 [IMAGE AVAILABLE] L18: 18 of 18
TITLE: I/O Subsystem using data link processors

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US PAT NO: 5,179,664 [IMAGE AVAILABLE] L19: 1 of 3
TITLE: Symbol-wide elasticity buffer with a read-only section and a read-write section

US PAT NO: 4,509,119 [IMAGE AVAILABLE] L19: 2 of 3
TITLE: Method for managing a buffer pool referenced by batch and interactive processes

US PAT NO: 3,665,421 [IMAGE AVAILABLE] L19: 3 of 3
TITLE: INFORMATION PROCESSING SYSTEM IMPLEMENTING PROGRAM STRUCTURES COMMON TO HIGHER LEVEL PROGRAM LANGUAGES

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US PAT NO: 5,519,345 [IMAGE AVAILABLE] L16: 1 of 2
TITLE: Reconfigurable interrupt device and method

DETDESC:

DETD(61)

In . . . urgent channel gets the next available cycle. However, the priority given in an automatic override is still lower than the **priority** of a **non-FIFO** request, such as refresh cycles.

US PAT NO: 5,510,740 [IMAGE AVAILABLE] L16: 2 of 2
TITLE: Method for synchronizing clocks upon reset

DETDESC:

DETD(61)

In . . . urgent channel gets the next available cycle. However, the priority given in an automatic override is still lower than the **priority** of a **non-FIFO** request, such as refresh cycles.

=>

US PAT NO: 5,561,807 [IMAGE AVAILABLE] L13: 1 of 15
TITLE: Method and device of multicasting data in a communications system

US PAT NO: 5,548,740 [IMAGE AVAILABLE] L13: 2 of 15
TITLE: Information processor efficiently using a plurality of storage devices having different access speeds and a method of operation thereof

US PAT NO: 5,548,587 [IMAGE AVAILABLE] L13: 3 of 15
TITLE: Asynchronous transfer mode adapter for desktop applications

US PAT NO: 5,329,579 [IMAGE AVAILABLE] L13: 4 of 15
TITLE: Modular adjunct processor made of identical multi-function modules adaptable under direction of one of them to perform any of the adjunct-processor functions

US PAT NO: 5,276,899 [IMAGE AVAILABLE] L13: 5 of 15
TITLE: Multi processor sorting network for sorting while transmitting concurrently presented messages by message content to deliver a highest priority message

US PAT NO: 5,006,978 [IMAGE AVAILABLE] L13: 6 of 15
TITLE: Relational database system having a network for transmitting colliding packets and a plurality of processors each storing a disjoint portion of database

US PAT NO: 4,956,772 [IMAGE AVAILABLE] L13: 7 of 15
TITLE: Methods of selecting simultaneously transmitted messages in a multiprocessor system

US PAT NO: 4,945,471 [IMAGE AVAILABLE] L13: 8 of 15
TITLE: Message transmission system for selectively transmitting one of two colliding messages based on contents thereof

US PAT NO: 4,825,438 [IMAGE AVAILABLE] L13: 9 of 15
TITLE: Bus error detection employing parity verification

US PAT NO: 4,814,979 [IMAGE AVAILABLE] L13: 10 of 15
TITLE: Network to transmit prioritized subtask pockets to dedicated processors

US PAT NO: 4,734,909 [IMAGE AVAILABLE] L13: 11 of 15
TITLE: Versatile interconnection bus

US PAT NO: 4,644,172 [IMAGE AVAILABLE] L13: 12 of 15
TITLE: Electronic control of an automatic wafer inspection system

US PAT NO: 4,543,630 [IMAGE AVAILABLE] L13: 13 of 15
TITLE: Data processing systems and methods

US PAT NO: 4,445,171 [IMAGE AVAILABLE] L13: 14 of 15
TITLE: Data processing systems and methods

US PAT NO: 4,412,285 [IMAGE AVAILABLE] L13: 15 of 15
TITLE: Multiprocessor intercommunication system and method

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US PAT NO: 3,654,621 [IMAGE AVAILABLE] L11: 1 of 1
TITLE: INFORMATION PROCESSING SYSTEM HAVING MEANS FOR DYNAMIC MEMORY ADDRESS PREPARATION

DETDESC:

DETD(31)

Having . . . checked associatively to see if the beginning of the new program segment to be executed is already resident in program **buffer** 44. **Nesting** and unnesting o
f PD control register 36 for procedure entry and
exit and loop control operators utilize PD control stack. . .

DETDESC:

DETD(105)

The **queue** and **variable-length queue** instructions are used for first-in first-out contiguous structures with fixed size and variable sized elements, respectively. Access to the first. . . either structure is made using the remove mode or enter mode, respectively. Element length is a parameter for accesses into **variable length queue** structures in enter mode. Accesses to both types of queue structures cause faults on queue full or empty conditions.

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US PAT NO: 5,568,639 [IMAGE AVAILABLE] L8: 1 of 5
TITLE: Method and apparatus for providing an object-oriented file structuring system on a computer

US PAT NO: 5,548,740 [IMAGE AVAILABLE] L8: 2 of 5
TITLE: Information processor efficiently using a plurality of storage devices having different access speeds and a method of operation thereof

US PAT NO: 5,524,268 [IMAGE AVAILABLE] L8: 3 of 5
TITLE: Flexible processor-driven control of SCSI buses utilizing tags appended to data bytes to determine SCSI-protocol phases

US PAT NO: 4,783,730 [IMAGE AVAILABLE] L8: 4 of 5
TITLE: Input/output control technique utilizing multilevel memory structure for processor and I/O communication

US PAT NO: 4,502,115 [IMAGE AVAILABLE] L8: 5 of 5
TITLE: Data processing unit of a microprogram control system for variable length data

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US PAT NO: 5,568,621 [IMAGE AVAILABLE] L1: 1 of 23
TITLE: Cached subtractive decode addressing on a computer bus

US PAT NO: 5,568,620 [IMAGE AVAILABLE] L1: 2 of 23
TITLE: Method and apparatus for performing bus transactions in a computer system

US PAT NO: 5,561,785 [IMAGE AVAILABLE] L1: 3 of 23
TITLE: System for allocating and returning storage and collecting garbage using subpool of available blocks

US PAT NO: 5,546,546 [IMAGE AVAILABLE] L1: 4 of 23
TITLE: Method and apparatus for maintaining transaction ordering and arbitrating in a bus bridge

US PAT NO: 5,535,340 [IMAGE AVAILABLE] L1: 5 of 23
TITLE: Method and apparatus for maintaining transaction ordering and supporting deferred replies in a bus bridge

US PAT NO: 5,533,205 [IMAGE AVAILABLE] L1: 6 of 23
TITLE: Method and system for efficient bus allocation in a multimedia computer system

US PAT NO: 5,506,969 [IMAGE AVAILABLE] L1: 7 of 23
TITLE: Method and apparatus for bus bandwidth management

US PAT NO: 5,485,586 [IMAGE AVAILABLE] L1: 8 of 23
TITLE: Queue based arbitration using a FIFO data structure

US PAT NO: 5,481,680 [IMAGE AVAILABLE] L1: 9 of 23
TITLE: Dynamically programmable bus arbiter with provisions for historical feedback and error detection and correction

US PAT NO: 5,471,632 [IMAGE AVAILABLE] L1: 10 of 23
TITLE: System for transferring data between a processor and a system bus including a device which packs, unpacks, or buffers data blocks being transferred

US PAT NO: 5,459,839 [IMAGE AVAILABLE] L1: 11 of 23
TITLE: System and method for managing queue read and write pointers

US PAT NO: 5,450,564 [IMAGE AVAILABLE] L1: 12 of 23
TITLE: Method and apparatus for cache memory access with separate fetch and store queues

US PAT NO: 5,432,920 [IMAGE AVAILABLE] L1: 13 of 23
TITLE: Store control method with hierarchic priority scheme for computer system

US PAT NO: 5,432,918 [IMAGE AVAILABLE] L1: 14 of 23
TITLE: Method and apparatus for ordering read and write operations using conflict bits in a write queue

US PAT NO: 5,398,325 [IMAGE AVAILABLE] L1: 15 of 23
TITLE: Methods and apparatus for improving cache consistency using a single copy of a cache tag memory in multiple processor computer systems

US PAT NO: 5,327,570 [IMAGE AVAILABLE] L1: 16 of 23

TITLE: Multiprocessor system having local write cache within each data processor node

US PAT NO: 4,965,716 [IMAGE AVAILABLE] L1: 17 of 23
TITLE: Fast access priority queue for managing multiple messages at a communications node or managing multiple programs in a multiprogrammed data processor

US PAT NO: 4,494,192 [IMAGE AVAILABLE] L1: 18 of 23
TITLE: High speed bus architecture

US PAT NO: 4,473,880 [IMAGE AVAILABLE] L1: 19 of 23
TITLE: Arbitration means for controlling access to a bus shared by a number of modules

US PAT NO: 4,305,124 [IMAGE AVAILABLE] L1: 20 of 23
TITLE: Pipelined computer

US PAT NO: 4,208,714 [IMAGE AVAILABLE] L1: 21 of 23
TITLE: Apparatus for giving priority to certain data signals

US PAT NO: 3,820,079 [IMAGE AVAILABLE] L1: 22 of 23
TITLE: BUS ORIENTED, MODULAR, MULTIPROCESSING COMPUTER

US PAT NO: 3,761,879 [IMAGE AVAILABLE] L1: 23 of 23
TITLE: BUS TRANSPORT SYSTEM FOR SELECTION INFORMATION AND DATA

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